IN THE CLAIMS

Presented below is a complete listing of all the claims in the format as permitted by the PTO waiver of 37 CFR 1.121 in accordance with the Official Gazette Notice of February 25, 2003.

1. (Original) A method of forming a device comprising:

patterning a first oxide upon a substrate;

forming a first nitride spacer mask upon the first oxide;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask;

forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask; and

forming a gate layer over the plurality of channels, wherein each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

2. (Original) The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer.

3. (Original) The method according to claim 1, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer.

4. (Original) The method according to claim 1, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer.

5. (Original) The method according to claim 1, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing agate etch with the second nitride spacer masks.

6. (Original) The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks, and further comprising:

forming a gate oxide upon the plurality of channels.

7. (Original) The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 300 nm.

8. (Original) The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 320 nm.

9. (Original) The method according to claim 1, wherein the substrate is made by providing a silicon on insulator substrate, and wherein the plurality of channels comprises monocrystalline silicon channels.

10. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, and wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels.

D8 cont.

11. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, and wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels.

12. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein the trench is filled with a dielectric, and wherein the plurality of channels comprises a plurality of single-gate quantum wire field effect transistors.

13. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein each of the plurality of channels has a gate oxide layer disposed thereupon, and wherein the second nitride spacer mask is disposed between the channel and the gate layer.

Claim 14 has been canceled.

15. (Original) The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels, and wherein the substrate is part of a silicon on insulator structure.

DB Cont

16. (Previously Amended) A method of forming a device comprising:

patterning a first oxide layer having a first width upon a substrate;

forming a first nitride layer upon the first oxide layer and the substrate, wherein the first nitride layer has a first thickness that is less than the first width;

forming a first nitride spacer mask from the first nitride layer, wherein the first nitride spacer mask has a width about equal to the first nitride layer thickness;

forming a second oxide layer upon the first nitride spacer mask, wherein the second oxide layer has a second thickness that is less than the width of the first nitride spacer mask;

forming a first oxide spacer mask from the second oxide layer, wherein the first oxide spacer mask has a width about equal to the second oxide layer thickness;

forming a second nitride layer upon the first oxide spacer mask, wherein the second nitride layer has a thickness that is less than the width of the first oxide spacer mask;

forming a second nitride spacer mask from the second nitride layer;

removing the first oxide spacer mask;

performing an etch over the second nitride spacer mask to form at least one semiconductor channel having a channel width and a length, wherein the mean free electron path therein is larger than the channel width;

forming a dielectric layer upon the channel length; and

forming a gate layer over the channel.

DB Amt.

17. (Previously Amended) The method according to claim 16, wherein the first oxide has a pitch of about three times the first width.

18. (Original) The method according to claim 16, wherein each performing a spacer etch comprises performing a reactive ion etch.

19. (Currently Amended) A ~~The~~ method ~~according to claim 16~~, ~~further~~ comprising:

forming a pattern of oxide structures upon a silicon layer, the oxide structures having a first width, the silicon layer overlying an insulator layer, and the insulator layer overlying a silicon substrate;

forming a first nitride spacer mask upon the first oxide structures;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask; and

performing an etch over the ~~patterned~~ second nitride spacer mask ~~that~~ to forms a silicon on oxide (SOI) ~~topology~~ structure ~~of~~ including a plurality of ~~semiconductor~~

~~channels~~ quantum wires formed from the silicon layer that are aligned to the second nitride spacer mask, the quantum wires being narrower than the mean free path of semiconductive electron flow therein. ~~wherein each of the plurality of semiconductive channels has a width of about one-tenth the first width;~~

~~forming an oxide upon the SOI topology; and~~

~~forming a gate layer over the oxide.~~

20. (Currently Amended) The method according to claim ~~16~~ 19, ~~further comprising:~~

~~performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than~~ wherein the first width of the oxide structures is approximately between 50nm to 200nm and the quantum wires have a second width that is about one-tenth the first width~~;~~

~~removing the patterned second nitride spacer mask;~~

~~forming an oxide upon the SOI topology; and~~

~~forming a gate layer over the oxide~~.

21. (Currently Amended) The method according to claim ~~16~~ 19, further comprising:

~~performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth the first width;~~

forming an oxide upon the ~~SOI topology~~ plurality of quantum wires;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic third width from about 2 times the first width to about 10 times the first width.

22. (Previously Amended) A method of forming a device comprising:

patterning a first oxide upon a substrate, wherein the first oxide has a characteristic width of X and a characteristic pitch selected from about 3X and about 3.2X;

forming a first nitride layer upon the first oxide, wherein the first nitride layer has a characteristic thickness of about one half X;

performing a spacer etch upon the first nitride layer and removing the first oxide to form a patterned first nitride spacer mask;

forming an oxide layer upon the patterned first nitride spacer mask, wherein the oxide layer has a characteristic thickness of about one fourth X;

performing a spacer etch upon the oxide layer and removing the patterned first nitride spacer mask to form a patterned first oxide spacer mask;

forming a second nitride layer upon the patterned first oxide spacer mask, wherein the second nitride layer has a characteristic thickness of about one-tenth X; and

performing a spacer etch upon the second nitride layer and removing the first oxide spacer mask to form a patterned second nitride spacer mask.

23. (Original) The method according to claim 22, further comprising:

performing an etch over the patterned second nitride spacer mask to form at least one semiconductor channel wherein the mean free electron path therein is larger than about one-tenth X.

24. (Original) The method according to claim 22, wherein X is in a range from about 20 nm to about 200 nm.

25. (Original) The method according to claim 22, wherein each performing a spacer etch comprises performing an reactive ion etch.

26. (Currently Amended) The method according to claim ~~22~~ 19, wherein the oxide structures further comprise a characteristic pitch of between about 3 to about 3.2 times the first width~~further comprising:~~

~~performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;~~

~~forming an oxide upon the SOI topology; and~~

~~forming a gate layer over the oxide~~.

27. (Cancel)

28. (Cancel)

39. (Currently Amended) A method of forming a structure comprising:

forming a plurality of semiconductive channels, each of the plurality of semiconductive channels comprising a channel length and a channel width, the plurality of semiconductive channels being formed by forming a first nitride spacer mask on an semiconductive layer, forming a first oxide spacer mask upon the first nitride mask, forming a second nitride spacer mask upon the first oxide spacer mask, and etching the plurality of semiconductive channels into the semiconductive layer in alignment with the second nitride spacer mask;

forming a dielectric layer upon the semiconductive channel length;

forming a source at a first terminal end of the plurality of semiconductive channels;

forming a second terminal end of the plurality of semiconductive channels;

forming a gate layer over the dielectric layer, wherein electron flow in the plurality of semiconductive channels has a mean free path that is greater than the semiconductive channel width, and wherein a first semiconductive channel of the plurality of semiconductive channels is spaced apart from a second semiconductive channel of the plurality of semiconductive channels by a trench that is less than about five times the semiconductive channel width.

40. (Previously Added) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric.

41. (Previously Added) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

42. (Previously Added) The method according to claim 39, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm.

43. (Previously Added) The method according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels upon a contact landing pad.

44. (Previously Added) The device according to claim 39, further comprising:

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

45. (Previously Added) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench.

DB cont.

46. (Previously Added) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact ahs a characteristic width in a range from about 200 nm to about 1,000 nm.

47. (Previously Added) The method according to claim 39, wherein forming a plurality of semiconductive channels comprises forming channels of monocrystalline silicon that is disposed upon a dielectric, wherein the semiconductive channel width is formed in a range from less than or equal to about 5 nm to about 30 nm and further comprising:

forming a self-aligned doping region in the monocrystalline silicon beneath the trench; and

forming a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

48. (New) A method, comprising:

forming a plurality of semiconductive channels into a first material, each of the plurality of semiconductive channels comprising a channel width having a mean free path smaller than electron flow, the plurality of semiconductive channels being formed by forming at least two spacer masks, the at least two spacer masks comprising second and third materials that can be etched with an etch chemistry selective to each other and also selective to the first material.

D8 Cont.

49. (New) The method of claim 48, wherein the first material is a silicon material, the second material is a nitride material, and the third material is an oxide material.

50. (New) The method of claim 48, further comprising:

forming the first spacer masks on the first material, each of the first spacer masks having a first width;

forming the second spacer masks along the sidewalls of the first spacer masks, each of the second spacer masks having a second width smaller than the first width of each of the first spacer masks;

etching the first spacer masks with an etch chemistry that entirely removes the first spacer masks but that does not etch the first material or the third material;

forming third spacer masks along the sidewalls of the second spacer masks, the third spacer masks also comprising the second material, each of the third spacer masks having a third width smaller than the second width of each of the second spacer masks, the third width being smaller than a mean free path of electron flow;

etching the second spacer masks with an etch chemistry that entirely removes the second spacer masks but that does not etch the first material or the third material; and

etching the first material in alignment with the sidewalls of the third spacer masks to form the plurality of semiconductive channels beneath the third spacer masks.